Form B

Princess Nora Bint Abdul Rahman University **Time: 60 minutes**
College of Computer and Information Sciences **Mid1**
CS 323 : computer architecture **Section No:**
Student Name: **ID:**

Question#1: Solve the following(5 marks):

1-) set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.

Answer:

1. The cache is divided into 16 sets of 4 lines each. Therefore, $16=2^4$
   Sets slot= 4 bit.

2. Main memory consists of $4K = 2^{12}$ blocks.
   the set plus tag lengths must be 12 bits
   tag length =12 – 4 = 8 bits.

3. Each block contains 128 words.
   $128=2^7$ 7 bits are needed to specify the word.

	S		
	Tag	**Sets slot**	**W**
Memory address	**8**	**4**	**7**

2-) Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size.

a. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

Answer:

Address Address format:

a. Tag = 20 bits it is given at question ;
b. 64-byte line = 2^6 , W=6 bits;
c. Number of addressable units = $2^{s+w} = 2^{32}$ = 4Gb ;
d. S=32-20=26
e. number of blocks in main memory = $2^s = 2^{26}$ = 67M blokcs;
f. r=26-20=6
g. Number of lines in cache = $2^r = 2^6 = 64$;
h. size of tag = 20 bits.

	S		
	Tag	**Cach line r**	**W**
Memory address=32	**20**	**6**	**6**

uestion#2(5 marks):

a) - How many **way** of input output techniques ? mention them ?

b) - explain one of them by flow chart?

Good luck

Ms.Bahiya