Form A

Princess Nora Bint Abdul Rahman University **Time: 15 minutes**
College of Computer and Information Sciences **Quiz-1**
CS 323 : computer architecture **Section No:**
Student Name: **ID:**

Question#1: Solve the following(5 marks):

1-) set-associative cache consists of 64 lines, or slots, divided into eight-line sets. Main memory contains 4K blocks of 256 words each. Show the format of main memory addresses.

Answer:

1. The cache is divided into 8 sets of = 64/ 8 = 8 lines each.
   Therefore, sets slote= 8 bits .

2. Main memory consists of 4K = 2^{12} blocks.

Therefore, the set plus tag lengths must be 12 bits .

3. therefore the tag length = 4 bits.
4. Each block contains 256 words. W =2^{8}

Therefore, 8 bits are needed to specify the word.

	S		
	Tag	**Sets slot**	**W**
Memory address	**4**	**8**	**8**

2-) Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size.

b. Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

b. Address format:
byte line = 64 =2^6 for that W= 6 bits.
Tag = 32-6 = 26 bits;
Number of addressable units = $2^{s+w} = 2^{32}$ bytes;
number of blocks in main memory = $2^s = 2^{26}$= 4Gb
Number of lines in cache = undetermined; size of tag = 26 bits.

	S= Tag	W
Memory address=32	**26**	**6**

Question#2(5 marks):

a) – mention the Interrupt Driven I/O basic Operation?

CPU issues read command
I/O module gets data from peripheral whilst CPU does other work
I/O module interrupts CPU
CPU requests data
I/O module transfers data

b) - explain simple interrupt flow chart?

Good luck

Ms.Bahiya